REMARKS

Claims 1-21 are pending in the present application and stand rejected. Claims 1, 9, 15-20 and 21 have been amended solely in response to the 35 U.S.C. § 112 rejection. The Examiner's reconsideration is respectfully requested in view of the following remarks.

Claims 1-21 stand rejected under 35 U.S.C. § 112, second paragraph. Applicants believe the claims are clear in light of the specification. For example, Figure 1(a) shows an exemplary module with two microprocessor units sharing a cache memory. The claims refer to "among cache memories," which implies more than one cache memory. Although Applicants do not agree with the Examiner's § 112 rejection, the rejected claims have been amended. Because the claims were amended solely in response to the § 112 rejection and to place the claims in better form, Applicants respectfully request entry of the amendments. Withdrawal of the claim rejections under 35 U.S.C. § 112 is respectfully requested.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Pong (U.S. Pub. No. 2002/0053004) (hereinafter "Pong"). The rejection is respectfully traversed.

Applicants maintain the arguments provided in the their Response on February 10, 2005, and additionally submit the following.

The Examiner cites the Abstract of Pong, and asserts that "shared memory" as taught by Pong anticipates "cache memory," as claimed in claim 1. This argument contradicts Pong itself and is entirely unreasonable even in basic computer science terminology. One skilled in the art would understand the difference between a shared memory and a cache memory in a conventional memory hierarchy. Cache memory is generally faster memory more closely tied to a particular processor.

Pong supports this last statement. Applicants point the Examiner to Figure 1 of Pong, which shows an exemplary shared memory system. As shown by Figure 1 of Pong, a first processor 102 has its own cache memory 116 and a second processor 104 has its own cache memory 118. Each processor 102, 104 shares a main memory 110 through a memory controller 130. A similar structure is shown in Figure 10(a) of the instant application. There is absolutely no basis for the Examiner to interpret "shared memory" as "cache memory," as the two are even distinguished within Pong.

The Abstract of Pong also states that "the [data] request may be broadcast, or specifically targeted to *processors having a copy of the requested data block.*" Implicitly, data blocks are stored within the cache memory of the processors.

Given the above, we now move on to "a plurality of processor modules." Claim 1 essentially claims that each processor module includes a cache memory and a plurality of processors sharing the cache memory. This is illustratively shown by Figure 1(a) of the instant application. Figure 1(a) shows an exemplary module A with two microprocessor units, MPU1 and MPU2, sharing a cache memory A.

Now, looking at Figure 1 of Pong, it is clear that the reference does not show even a *single* module, much less a *plurality* of modules. As shown in Figure 1, each processor has only one cache. Even assuming, *arguendo*, that the memory is a cache (which makes no logical sense since Pong uses the term "cache" explicitly), then Figure 1 shows only a *single* module.

In light of the above, Applicants request withdrawal of the claim rejection, or otherwise clarification of the logical inconsistencies of the Examiner's rejections presented above.

Claims 9, 11, 12, 15, 17, 18 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pong. In light of the arguments presented for claim 1, claims 9, 15 and 21 are believed to be patentably distinguishable and nonobvious over Pong.

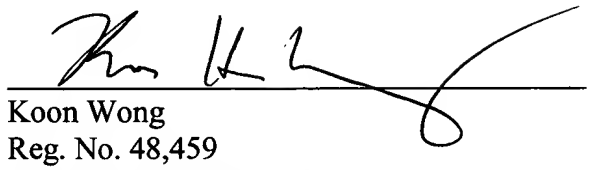
Other rejections include in the following. Claims 2-5, 10 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pong in view of Kaneko et al. (U.S. Patent No. 5,349,656) (hereinafter "Kaneko"). Claims 6-8, 14, and 19-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pong in view of Kaneko, and further in view of Barajas et al. (U.S. Patent No. 5,598,551) (hereinafter "Barajas"). Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Pong in view of Barajas.

Dependent claims 2-8 are believed to be allowable for at least the reasons given for independent claim 1. Withdrawal of the rejection of claims 1-8 under 35 U.S.C. § 102(e) is respectfully requested.

Dependent claims 10-14 and 16-20 are believed to be allowable for at the least the reasons given for independent claims 9, 15 and 21. Withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

By: 

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